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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/800,510	03/15/2004	Tien-I Bao	TSM03-0927	9453

43859 7590 03/02/2006

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EXAMINER	
HO, TU TU V	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 03/02/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/800,510	BAO ET AL.	
	Examiner	Art Unit	
	Tu-Tu Ho	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 December 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *24,25 and 27-43* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *24,25 and 27-43* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 January 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Applicant's Amendment filed 12/02/2005 and formal drawing submitted on 01/17/2006 have been reviewed and placed of record in the file.

2. Applicant's arguments with respect to claims 24-25 and 27-43, filed 12/02/2005, have been considered but they are moot in view of new ground(s) of rejection.

3. Summary of terms defined and arguments provided:

3.t Thin: Applicant has confirmed that the limitation "thin" in the "thin stop layer" of claim 24 is defined as "about 300Å and less" (Argument filed 07/01/2005, page 8; specification, paragraph [0008]);

3.fod Substantially free of damage: "Substantially free of damage" as used in the invention and in the claimed invention, as applied to a method for processing a semiconductor structure defining a metallization layer (14, Fig. 2A, present invention) which results in said metallization layer being substantially free of damage (said method comprising capping a top surface of said semiconductor structure that defines said metallization layer with a thin stop layer (32), forming a layer (18) of dielectric over said layer of thin stop, said layer of dielectric defining at least one area (38) where said thin stop layer (32) is exposed, and removing said exposed thin stop layer to expose a top surface of said metallization layer (14) which is substantially free of damage), implies not only that said thin stop layer has a thickness range of about 100 Å to about 300Å but also that said removing said exposed thin stop layer to expose a

top surface of said metallization layer includes removing said exposed thin stop layer according to said thickness range (specification, present invention, Applicant's Remarks and Affidavits, filed 07/01/2005 and 12/02/2005).

Claim Rejections - 35 USC § 102

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

4. **Claims 24-25, 27, 31, 33, and 42-43** are rejected under 35 U.S.C. 102(b) as being anticipated by Wang et al. U.S. Patent 6,146,987 (the '987 reference).

The '987 reference discloses in Figures 3-7 and respective portions of the specification a method of fabricating semiconductor device as claimed.

Referring to **claim 24,** the reference discloses a method for processing a semiconductor structure defining a metallization layer (303, Fig. 3) which inherently results in said metallization layer being substantially free of damage comprising the steps of:

capping a top surface of said semiconductor structure that defines said metallization layer with a thin stop layer (401, col. 2, lines 54-61; "thin" is interpreted according to Application's definition, see paragraph numbered 3 above);

forming a layer (403) of dielectric over said layer of thin stop, said layer of dielectric defining at least one area (503, Fig. 5) where said thin stop layer (401) is exposed; and

removing said exposed thin stop layer to expose a top surface of said metallization layer (303, Fig. 6) which is inherently substantially free of damage (see paragraph numbered 3 above for the limitation "substantially free of damage").

In re **claim 25**, the '090 patent further discloses that said step of forming a layer of dielectric comprises forming a patterned layer of dielectric according to a patterned layer of resist (501, Fig. 5), said pattered layer of dielectric defining a layout for an upper layer of metallization (703, Fig. 7), and said step of removing further comprises removing said patterned layer of resist (501, Figs. 6-7).

Referring to **claim 42** and using the same references, citations, and interpretations as detailed above for claim 24 where applicable, the reference discloses a method of forming the layout for an upper level of metallization (703) in a semiconductor with inherently reduced damage to a lower level of metallization (303) comprising the steps of:

providing a substrate (305/301) having a surface, said surface including a top surface of said lower level of metallization;

capping said lower level of metallization with a stop layer deposited to a thickness in the range of approximately 100 - 100Å, which range is inside the claimed range of less than 300Å, over said surface;

forming a patterned layer of dielectric over said etch stop layer according to a patterned layer of resist on said dielectric layer, said patterned dielectric layer defining said layout for an upper level of metallization, and said layout including at least one area where said etch stop layer is exposed; and

removing said patterned resist and said exposed etch stop layer to expose, inherently substantially damage free, a portion of said top surface of said lower level of metallization.

Referring to **claim 43**, and using the same references, citations, and interpretations as detailed above for claims 24 and 42 where applicable, the reference discloses a method of

forming an upper level of metallization in a semiconductor device with reduced damage to a lower level of metallization comprising the steps of:

providing a substrate having a top surface, said top surface defining said lower level of metallization;

capping said lower level of metallization with a stop layer deposited to a thickness in the range of approximately 100 - 200Å, which range is inside the claimed range of less than 300Å, over said surface;

depositing a layer of inter-metal dielectric (IMD) (403) over said stop layer;

depositing and patterning a layer of resist to define a patterned mask over said layer of a IMD;

etching said layer of IMD to remove material according to said mask, said removed material defining the layout for an upper level of metallization, and said layout including at least one area where said layer of IMD is completely etched through to expose said stop layer;

removing said patterned resist and said exposed stop layer; and

filling said layout etched in said IMD layer with metal (703) to form said upper layer of metallization.

Referring to **claim 27**, the reference further discloses that said thin stop layer is deposited to a thickness of about 100-200 Å (col. 2, lines 54-60), which is less than 300 Å as is generally defined in the specification of the present invention and which meets the claimed thickness of about 100 Å.

Referring to **claim 31**, the material list of the reference (SiN "silicon nitride", col. 2, lines 53-60) for the thin stop layer meets the requirement of the claimed group of materials.

Referring to **claim 33**, the process for forming the thin stop layer (CVD, col. 2, lines 53-60) disclosed by the reference meets the requirement of the claimed group of processes.

Claim Rejections - 35 USC § 103

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

5. **Claims 28 and 34** are rejected under 35 U.S.C. 103(a) as obvious over Wang et al. U.S. Patent 6,146,987 (the '987 reference).

Referring to **claim 28**, the reference discloses that the step of filling said layout etched in said dielectric layer with a conductive metal, such as tungsten (703, column 3, lines 25-28). Although the reference does not disclose that the tungsten layer 703, which is a conductive layer, may be copper, which is a conductive layer, changing said conductive layer to another conductive layer would have been obvious to one of ordinary skill in the art at the time the invention was made because the reference does not prelude such changing of conductive materials.

Referring to **claim 34**, the reference discloses that said thin stop layer is deposited by CVD as mentioned above. Although not disclosed, said CVD process is performed at a temperature. Although the reference does not teach that said temperature is between about 200°C and about 500°C as claimed, the reference also does not disclose that said CVD is performed at a high temperature. Hence, it is reasonable to conclude that said CVD is performed at a temperature that is not a high temperature, which is also known in the art as a low-temperature process, which is between about 200°C and about 500°C as claimed.

6. **Claims 29-30 and 32** are rejected under 35 U.S.C. 103(a) as obvious over Wang et al. U.S. Patent 6,146,987 (the '987 reference) in view of Kloster et al. U.S. Patent Application Publication 20020140103 (the '103 reference).

The '987 reference discloses a method for forming a metalization layer for a semiconductor structure substantially as claimed and as detailed above for claim 24 including said etch stop layer, but does not disclose that said etch stop layer is a multilayered layer, and does not disclose the materials as claimed in claims 29 and 30 (organic and containing a metal) for the etch stop layer.

Kloster, in disclosing a method for forming a metalization layer for a semiconductor structure (Fig. 1) including an etch stop layer 16/18, teaches that said etch stop layer 16/18 should be a multilayered layer (16 and 18), and further teaches materials as claimed in claims 29 and 30 (organic and containing a metal, paragraphs [0023], [0026], and [0028]), so as to reduce RC delay in said semiconductor structure (paragraph [0016]).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the '103 reference's structure such that said thin etch stop layer is a multilayered layer. One would have been motivated to make such a change in view of the teachings in Kloster that such a change, which also supplies the available and known materials, leads to reduced RC delay in said semiconductor structure.

7. **Claims 35-41** are rejected under 35 U.S.C. 103(a) as obvious over Wang et al. U.S. Patent 6,146,987 (the '987 reference) in view of Cohen U.S. Patent Application Publication 20040087171 (the '171 reference).

The '987 reference discloses a method for forming a metalization layer for a semiconductor structure including a semiconductor substrate substantially as claimed and as detailed above for claim 24 including, for forming said semiconductor substrate, depositing a dielectric layer 305, forming a trench in said dielectric layer, depositing a metal (303) in said trench, but does not disclose forming a metal seed layer in said trench before depositing said metal. The reference further does not disclose forming a barrier layer over the trench prior to forming said seed layer (in re claim 36), and thus also does not disclose that said forming said metal seed layer comprises forming a first metal seed layer and a second metal seed layer over said first metal seed layer (in re claim 38) and the required materials, processes, and characteristics as recited in claims 37 and 39-41.

Cohen, in disclosing a method for forming a metalization layer in a trench for a semiconductor structure, teaches that (1) forming a barrier layer prior to forming a seed layer to provide good adhesion to the layer that forms the trench for the metallization layer (paragraph [0005], (2) forming a first and second metal seed layer to provide a low-resistance electrical path and to provide a void-free metalization layer for the metalization layer (paragraphs [0003], [0014], and [0015]).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the '987 reference's device such that forming said semiconductor substrate includes forming a metal seed layer in said trench before depositing said metal, forming

a barrier layer over the trench prior to forming said seed layer, and forming said metal seed layer comprises forming a first metal seed layer and a second metal seed layer over said first metal seed layer. One would have been motivated to make such a change in view of the teachings in Cohen that such a change results in good adhesion to the layer that forms the trench for the metallization layer, a low-resistance electrical path, and a void-free metalization layer for the metalization layer.

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tu-Tu Ho whose telephone number is (571) 272-1778. The examiner can normally be reached on 6:30 am - 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, DAVID NELMS can be reached on (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tu-Tu Ho
February 23, 2006